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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,194	11/02/2001	Ketankumar B. Patel	01CON231P	4343

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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,194	PATEL, KETANKUMAR B.	
	Examiner	Art Unit	
	Walter F Briney III	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1-3, 5, 10-12, 15, 16, 19, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Okada (US Patent 5,425,096).**

Claim 1 is limited to *a DC driver circuit coupled to a tip/ring line*. Okada discloses a communication device. See Abstract. Figure 2 depicts a schematic representation of the device, and in particular, a schematic of a DC termination circuit for a modem. The circuit includes a line holding *amplifier* (95). The amplifier is connected to a rectified *tip/ring* signal, which is generated by diode bridge (96), through a first transistor (93) (i.e. *a first switch*). The first transistor being connected to a *first capacitor* (C1). Okada discloses *an RC circuit* (C2, R6), which is selectively charged in response to transistor (94) (i.e. *a second switch*). Both the RC and amplification circuits are coupled to the second transistor (94) by way of the first transistor (93). Furthermore, the first transistor, the RC circuit, and the amplifier are connected at node D (i.e. *wherein said RC circuit, said first switch, and said amplification circuit share a common node*). It follows that the rate of discharge at that node can inherently be adjusted by changing the component values. Attention is now drawn to figure 3, wherein it is made clear that transistors (93) and (94) operate in the same states at the same times. Therefore,

when transistor (93) is closed, thus allowing current to be drawn by the amplifier (95), transistor (94) is closed and clearly the converse holds. Therefore, Okada anticipates all limitations of the claim.

Claim 2 is limited to *the DC driver circuit of claim 1*, as covered by Okada. Okada discloses a third transistor (91), which operates in the complimentary fashion as transistors (93) and (94), such that it is closed during a *break state*, and causes the first capacitor (C1) to charge to the level of the virtual ground (i.e. *further comprising a third switch having a first terminal coupled to a voltage source and a second terminal coupled to said first capacitor, said third switch being closed during said break state to precharge said first capacitor*). Therefore, Okada anticipates all limitations of the claim.

Claim 3 is limited to *the DC driver circuit of claim 1*, as covered by Okada. As is clear from figure 2, capacitor (C2) of the RC circuit is connected to the amplifier (95) at node D, and is connected to a virtual ground at its other terminal (i.e. *wherein said second capacitor has a first terminal coupled to said amplification circuit and a second terminal coupled to ground*). Therefore, Okada anticipates all limitations of the claim.

Claim 5 is limited to *the DC driver circuit of claim 1*, as covered by Okada. As is clear from figure 2, resistor (R6) of the RC circuit is connected to the amplifier's base (95) at one terminal and to the virtual *ground* at the other terminal (i.e. *wherein a resistor of said RC circuit has a first terminal coupled to said amplification circuit and a second terminal coupled to ground*). Therefore, Okada anticipates all limitations of the claim.

Claim 10 is limited to *the DC driver circuit of claim 1*, as covered by Okada. As indicated in the rejection of claim 1, the DC termination circuit of Okada is adapted for use with a modem (i.e. *wherein said tip/ring line is coupled to a modem*). See figure 2. Therefore, Okada anticipates all limitations of the claim.

Claim 11 is limited to a circuit for reducing a peak voltage at a selected line. Okada discloses a communication device, the device includes a DC holding transistor (95), which is selectively driven by one of a first capacitor (C1) or a second capacitor (C2), which is part of an RC circuit. During a make state, C1 holds the voltage at node A to a level higher than the level at the emitter of transistor (94). This causes current to flow through said transistor, which in turn activates transistor (93), which then activates transistor (95). During a break state, C1 is short-circuited with the virtual ground, forcing node A to even out with the level of the emitter of transistor (94). This causes current to cease flowing through said transistor, which in turn deactivates transistor (93), which ceases telephone line current from supplying transistor (95). Transistor (95) remains conductive for an amount of time that is proportional to the time constant of capacitor C2 and R6. The effect of the RC circuit is to prevent transistor (95) from spontaneously closing, thus collapsing the current path therethrough, and causing voltage transients at the modem interface. As indicated in the rejection of claim 1, the RC circuit, first switch and amplifier share a common node, and changes to any of the components will inherently affect the discharge rate. Therefore, Okada anticipates all limitations of the claim.

Claim 12 is limited to the circuit of claim 11, as covered by Okada. As is clear from figure 2, Okada is driving a tip/ring line, which is produced as an output from diode bridge (96) (i.e. *wherein said selected line is a tip/ring line*). Therefore, Okada anticipates all limitations of the claim.

Claim 15 is limited to the circuit of claim 11, as covered by Okada. Transistor (93) (i.e. *said first switch*) has been shown in the rejection of claim 11 to cause the amplifier (95) to be driven by current from a tip/ring line. Therefore, Okada anticipates all limitations of the claim.

Claim 16 is limited to the circuit of claim 15, as covered by Okada. Transistor (94) (i.e. *a second switch*) has been shown in the rejection of claim 11 to cause the amplifier (95) to be powered by the RC circuit during a break state. Therefore, Okada anticipates all limitations of the claim.

Claim 19 is essentially the same as claim 2, and is rejected for the same reasons.

Claim 21 is essentially the same as claim 10, and is rejected for the same reasons.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada.

Claim 4 is limited to *the DC driver circuit of claim 3*, as covered by Okada. Okada does not disclose the relative sizing of capacitor (C1) and capacitor (C2). Therefore, Okada anticipates all limitations of the claim with the exception *wherein said first capacitor has a first capacitance value that is substantially greater than a second capacitance value of said second capacitor.*

Analysis of the circuit depicted in figure 2 suggests that capacitor (C2) must quickly lock and maintain a DC loop. In fact, Okada provides a photocoupler (92) for the purpose of enabling the quick charging of capacitor (C2), which would suggest that it would have been obvious to one of ordinary skill in the art at the time of the invention to choose the smallest capacitance value that still rejects enough AC signals to be operable. Capacitor (C1), however, does not include the fast-charging circuit of capacitor (C2). This suggests that the value of (C1) should be balanced more critically between speed-of-response and AC signal rejection, which suggests a larger size than capacitor (C2). It would have been obvious to select a first capacitor, whose capacitance is significantly greater than a second capacitor based on the design choices illustrated above.

Claim 18 is essentially the same as claim 4, and is rejected for the same reasons.

3. Claims 6-9, 13, 14, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada in view of Yurgelites (US Patent 5,500,895).

Claim 6 is limited to *the DC driver circuit of claim 1*, as covered by Okada. The disclosure of Okada includes a simplistic line holding transistor (95). Use of a single device often effects the stability and efficiency of the device. Therefore, Okada anticipates all limitations of the claim with the exception *wherein said amplification circuit comprises an op-amp coupled to a first transistor.*

In order to mitigate the stability problems of a single-ended amplifier without any feedback, many designers have employed a voltage-controlled current supply, like that shown in Yurgelites. In particular, the circuit (78) of figure 9 includes an op-amp that is coupled to a representative line voltage (V_L), and uses that reference value to drive a pair of current sources, depicted as coupled transistors. The op-amp's stability and accuracy is maintained through feedback. It would have been obvious to one of ordinary skill in the art at the time of the invention to employ a voltage-controlled current source as taught by Yurgelites for the purpose of improving the stability and robustness of the DC current sink of Okada.

Claim 8 is limited to *the DC driver circuit of claim 6*, as covered by Okada in view of Yurgelites. As the operation is to be the same, even with the addition of the teachings of Yurgelites, the first transistor will draw current in a make state, and be prevented from drawing current during a break state. Therefore, Okada in view of Yurgelites makes obvious all limitations of the claim.

Claim 7 is limited to *the DC driver circuit of claim 1*, as covered by Okada. For the same reasons as claim 6, it would have been obvious to combine the teachings of Yurgelites with the device of Okada. As seen in figure 9, the new holding circuit

includes *an op-amp* and *a first* and *second transistor*. Therefore, Okada in view of Yurgelites makes obvious all limitations of the claim.

Claim 9 is limited to *the DC driver circuit of claim 7*, as covered by Okada in view of Yurgelites. As the operation is to be the same, even with the addition of the teachings of Yurgelites, the first and second transistor will draw current in a make state, and be prevented from drawing current drawing a break state. Therefore, Okada in view of Yurgelites makes obvious all limitations of the claim.

Claim 13 is limited to the circuit of claim 11, as covered by Okada. For the same reasons as claim 6, it would have been obvious to combine the line holding amplifier arrangement as taught by Yurgelites with the device of Okada (i.e. wherein said at least one transistor is driven by an op amp). Therefore, Okada in view of Yurgelites makes obvious all limitations of the claim.

Claim 14 is limited to the circuit of claim 13, as covered by Okada in view of Yurgelites. The operation of the device remains the same, even with the addition of the op-amp taught by Yurgelites. Thus, said op amp is driven by said first capacitor when said circuit is in said make state. Therefore, Okada in view of Yurgelites makes obvious all limitations of the claim.

Claims 17 and 20 describe an arrangement that is essentially the same as claims 3 and 5, respectively, and are rejected for the same reasons.

Response to Arguments

Applicant's arguments with respect to claims 1-21, filed 15 June 2004, have been considered but are moot in view of the new ground(s) of rejection.

The rejections of claims 4 and 8 under 35 U.S.C. 112 second paragraph have been sufficiently overcome by the applicant's amendments. The rejections have been withdrawn .

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F Briney III whose telephone number is 703-305-0347. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
11/10/04

XU MEI
PRIMARY EXAMINER